REMARKS

As a preliminary matter, Applicants have made minor grammatical changes to several of the claims. Applicants submit that the claims are now in condition for allowance, such action is respectfully requested.

Claims 1 and 5 stand rejected over Shimada et al. (U.S. Patent No. 5,056,116) in view of Byrne et al. (U.S. Patent No. 6,487,672), and further in view of Sprague (U.S. Patent No. 6,072,645). Claims 2, 6-8, 12-13 stand rejected over the references as applied to claims 1 and 5, and also in view of Leung et al. (U.S. Patent No. 6,564,518). Claim 4 stands rejected over the same references as claims 1 and 5, and also in view of Zook (U.S. Patent No. 5,600,662). Claims 9-11 stand rejected over the same references applied to claims 1 and 5, and also in view of Bushy, Jr. (U.S. Patent No. 4,896,337) and further in view of Scheffler (U.S. Patent No. 5,041,921)). Further, claims 14-17 stand rejected over the references as applied to claims 1 and 5, and further in view of Bushy, Jr., Scheffler, and Leung.

Applicants traverse all of the rejections of all the claims because the cited references do not disclose or suggest an apparatus with "a first clock signal generating part generating a first clock signal, and a second clock signal generating part generating a second clock signal different from the first clock signal" where the first clock signal is associated with "sampling a read signal from recorded data of a recording medium" and the second clock signal is associated with "a data detecting part retrieving the sample value from the first storing part" as in all amended independent claims 1, 4, 5, 12, 13, 14 and 16. In other words, the references do not disclose or suggest an apparatus that includes two clock signal

generating parts (PLL 17 and synthesizers 32 and 47) for generating different clock signals (first and second clock signals) so that the read system and the detection system can be independently operated (See FIG. 3 and FIG. 4).

Shimada does not disclose these features because both CLK1 and CLK2 are used for sampling (FIG. 24 and FIG. 26, Col. 19, line 40 to Col 20 line 2). Shimada merely discloses a process clock, CLK1, which is used as a sampling clock, and a process clock for sampling, CLK2, which has a half frequency of the process clock CLK1. The CLK2 of Shimada is merely associated with the digital phase locked loop circuit 11, the rate converter circuit 13, and the data decoding circuit 14, which operate based on the processing clock CLK2 (col. 19, lines 30-40, FIG. 22). The CLK2 of Shimada is not associated with a data detecting part (FIG. 22). Further, Shimada is not directed to improving the Signal to Noise Ratio and improving density of the recorded data, nor is it directed to a read system and a detection system that can be independently operated, as in the present invention. Thus, Shimada does not disclose or suggest the features of all amended independent claims 1, 4, 5, 12, 13, 14 and 16.

Byrne does not remedy the deficiencies of Shimada. Byrne also does not apply a first clock signal for sampling a read signal from recorded data and a second clock signal for retrieving the sample value from the first storing part in a data detecting part. Byrne merely discloses a configuration to supply adjusted sampling data to a detector.

Sprague does not remedy the deficiencies of Byrne and Shimada, and is merely directed to a recording device, such as an audio tape recorder, in which the recent past is

temporarily recorded in a memory until the user can select a retroactive start time to record the data onto a medium. In the retroactive recording device of Sprague, past information is temporarily stored in a solid state retroactive memory, and based on a selection of buttons by the user, such as "START A," "START B," AND "START C," the retroactive recording device transfers the past information to the audio tape. Since the retroactive recording device of Sprague is a recording device, and not a device to read data from a recording medium, even if the data demodulation apparatus of Shimada and the retroactive recording device of Sprague are combined, features of the present invention cannot be achieved. Shimada and Sprague do not disclose the configuration of two clock signal generating parts generating different clock signals so that the read system and the detection system can be independently operated.

Further, each additional reference does not remedy the deficiencies of Shimada, Byrne and Sprague, but are cited for a particular additional feature in each claim. Applicants submit that none of these references taken alone or in combination, disclose or suggest the invention as claimed.

Leung is merely cited for disclosing "an apparatus data detecting part having a recursive process conducting part conducting a recursive process for the sample data retrieved from the first storing part in accordance with the predetermined algorithm so that maximum likelihood data is detected." However, Leung is a detector error suppression circuit that is used to remove single bit errors by comparing samples to detected EPR4 bits, not a recursive process that is synchronized with a second clock signal which is faster than a

first clock signal for increasing the speed of recursive detection. Further, Leung cannot realize improved Signal to Noise Ratio and improved density of the recorded data as in the present invention.

Bushy is cited for disclosing an apparatus that has two different memory devices that receive data and that switch between the memory devices. However, Bushy merely discloses a configuration to adjust the frequency of successive data, the configuration utilizing two memories, an input memory and an output memory. The input memory receives input data at a high frequency, while simultaneously the output memory outputs the stored data at a low frequency. In the present application, however, the sampling data is written in to the FIFO memory and the sampling data is read out from the FIFO memory to be used for recursive detection. One FIFO memory stores the MO data and another FIFO memory stores the ID.

Scheffler is cited for teaching a second storing part that consecutively stores a sample value obtained by a sampling part. Scheffler is merely directed to a system for recording custom albums from a library of pre-recorded items and does not address increasing the speed of recursive detection.

Zook is cited for disclosing the feature of storing address data. However, Zook is merely directed to an error correction apparatus that corrects an error burst occurring in the header information such as the sector ID data, and is not directed to increasing the speed of recursive detection.

Neither the primary references Shimada, Byrne nor Sprague, and additionally Leung et al., Zook, Bushy and Scheffler, disclose an apparatus that applies a first clock signal associated with "a sampling part for sampling a read signal from recorded data of a recording medium by synchronizing with a first clock signal," and a second clock signal associated with "a data detecting part retrieving the sample value from the first storing part by synchronizing with a second clock signal," as in all independent claims 1, 4, 5, 12, 13, 14 and 16.

It is submitted that the question under 35 U.S.C. §103 is whether the totality of the art would collectively suggest the claimed invention to one of ordinary skill in this art. The test is whether the invention as a whole, in light of all of the teachings of the references in their entireties, would have been obvious to one of ordinary skill in the art at the time the invention was made. It is insufficient that the art disclosed components of Applicants' invention, either separately or used in other combinations. A teaching, suggestion, or incentive must exist to make the combination made by Applicants. In this case, there is absolutely no incentive in the references to combine. Moreover, even if, arguendo, such an incentive existed, the combination of references would not result in an apparatus applying the first clock signal associated with "a sampling part for sampling a read signal from recorded data of a recording medium by synchronizing with a first clock signal," and a second clock signal associated with "a data detecting part retrieving the sample value from the first storing part by synchronizing with a second clock signal," as in all independent claims 1, 4, 5, 12, 13,

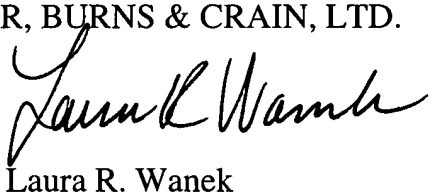
14 and 16. Accordingly, Applicants submit the rejections of all the claims have been overcome and should be withdrawn.

Furthermore, none of the cited prior art references considered the problem faced and solved by the present inventor, that of simultaneous processing of the read process in the read system, and the detection process in the detection system. Accordingly, Applicants submit the rejections of all the claims have been overcome and should be withdrawn.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. Should the Examiner be of the opinion that a telephone conference would aid in the prosecution of the application, or that outstanding issues exist, the Examiner is invited to contact the undersigned.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

Laura R. Wanek
Registration No. 53,737

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300 South Wacker Drive - Suite 2500
Chicago, Illinois 60606
Telephone: (312) 360-0080
Facsimile: (312) 360-0080
Customer No. 24978
P:\DOCS\0941\65368\442839.DOC